



1. General:

The FD77 oscillator has many options available to simplify and enhance system design. The FD77 contains five independent frequency generators, driving seven output pins in a very small 5x7mm ceramic package. These frequency generators are comprised of one reference oscillator and four M/N PLL blocks. In addition to fixed frequencies, optional spread spectrum modulation is available within the PLL blocks. In the event that all seven outputs are not required, unused outputs may be disabled.

This application note is a guide to capturing system requirements so that the FD77 may be configured to your specific application. To complete the process, enter your requirements in the table 1 and forward it to your Pletronics representative.

2. FD77 Features:

For reference, a block diagram of the FD77 is shown in figure 1.

Power Supply: The FD77's power supplies are not part of the configuration program but there are choices. The FD77's logic core is supplied from a 1.8v $\pm 5\%$ source. The interface logic is supplied from a power source of 2.5v or 3.3v to match your system I/O requirements.

Reference Oscillator: This crystal oscillator is the heart of the FD77 and is used to generate all of the outputs from the FD77. The standard reference oscillator frequency is 25MHz. This frequency may be especially useful for Ethernet applications. Standard tolerance, is 50ppm but 25ppm and 20ppm are also available. For custom applications, frequencies between 12MHz and 32MHz may be specified.

Output 1: This output is a sub-multiple of either the reference oscillator or PLL block 1. The selected input is divided by a 10-bit divider to yield the final frequency for output 1. Values for this divider range from 1 to 1023. When the reference oscillator is used as its input, Output 1 has slightly better jitter performance which would be appropriate for jitter sensitive applications. The frequency range for output 1 is 12KHz to 230MHz.

Table 1 Input: Please indicate the desired frequency for Output 1 on table 1.

Output 2 thru 7: These outputs are derived from four PLL blocks and six output dividers within the FD77. These PLL blocks and dividers implement general purpose M/N frequency synthesizers.

Table 1 Input: For each output, indicate the frequency required in table 1. Un-needed outputs will be disabled.

In addition to a frequency synthesizer, each PLL block contains a spread spectrum modulator. This feature, if enabled, modulates the output frequency to reduce EMI effects. Spread spectrum modulation may be down or centered. Modulation deviation is selectable in .25% steps from 0 to 2%.

Table 1 Input: For each output indicate if spread spectrum is required.

Table 1 Input: For each output requiring spread spectrum, indicate if you require down spread or centered spread.

Table 1 Input: For each output requiring spread spectrum, indicate the modulation percentage required. Valid selections are 0.25%, 0.5%, 0.75%, 1.0%, 1.25%, 1.5%, 1.75% and 2.0%.

FD77 Customer Specifications

3. Requirements:

Table 1				
Resource	Output Frequency	Spread Spectrum	Spread D/C	Spread Modulation %
Reference	25.0 MHz	N/A	N/A	N/A
Output A				
Output B				
Output C				
Output D				
Output E				
Output F				
Output G				

Notes:

Output designations in table 1 have been changed from number designators to letters. This is intentional. There are many ways to generate the required frequencies. During the configuration process, Pletronics will assign outputs as needed to satisfy these requirements.

Complete this section and submit requirements to ple_sales@pletronics.com	
Customer Name	
Application/Project Name	
Estimated Annual Usage	
# of samples required	
Part Number (Pletronics to complete)	