

OeD4
3.2 x 5.0 x 1.50 mm
LCC Ceramic Package

Features

- Pletronics' OeXO® Series Ovenized equivalent Temperature Compensated Crystal Oscillator
- Optional Voltage Control Function
- Low Power / Fast Warm Up
- CMOS or Clipped Sine Wave Output
- 2.8V to 3.3V nominal Supply Voltage
- See table for developed Frequencies

Applications

SONET / SDH / DWDM
Test & Measurement
Telecom Transmission & Switching Equipment
Base Stations / Picocell
Wireless Communication Equipment

Electrical Characteristics for CMOS

Parameter	Min	Typ	Max	Unit	Condition (Consult factory for other options)
Frequency Range ²	8.192	-	40.0	MHz	See table below for developed frequencies
Frequency Stability vs. Temperature ²	-200 -100 -50	-	+200 +100 +50	ppb	Over -40°C to +85°C Over -10°C to +70°C Over 0°C to +70°C at fixed V _{CC} + load (reference to midpoint min/max frequency) See factory for other options
Frequency Initial Calibration		-	±2.0	ppm	V _{control} 1.50 volts at 25°C ± 2°C when V _{CC} ≥ 2.8 volts If V _{control} used
Operating Temperature Range ²	-40	-	+85	°C	Widest range available
Supply Voltage ^{1,2} V _{CC}	2.8	-	3.3	Volts	± 5%
Supply Current ² I _{CC}	-	2.0 3.0 4.0	-	mA	13 MHz 26 MHz 40 MHz Load: 15 pF, V _{CC} ± 5%
Frequency Stability vs. Supply	-	-	±0.2	ppm	Load: 15 pF, V _{CC} ± 5%
Frequency Stability vs. Load	-	-	±0.2	ppm	Load: 15 pF ± 10%
V _{control} Range	0.5	-	2.5	Volts	1.50 volts nominal for V _{CC}
Frequency Pullability ²	0	±8.0	±12.0	ppm	Positive Slope
Linearity	-	-	2.0	%	
Output Waveform	CMOS				
Duty Cycle	40	50	60	%	Load: 15 pF
Output V _{HIGH}	90	-	-	%V _{DD}	V _{th} : T _R and T _F 10% and 90% of amplitude V _{th} : D.C. 50% of amplitude
Output V _{LOW}	-	-	10	%V _{DD}	
Output T _{RISE} and T _{FALL}	-	-	6.5	nS	
Startup Time	-	-	10.0	mS	Within ± 2.0 ppm of final frequency
Long Term Stability (Aging)	-	-	±1.0	ppm	Per year at 25°C ± 2°C
Phase Noise	100 Hz 1 kHz 10 kHz 100 kHz	-	-120 -134 -144 -145	-	dBc/Hz 25°C ± 2°C at 20.0 MHz
Jitter	-	0.6	-	pS	Frequency offset from carrier 12 kHz to 20 MHz, Typical performance at 20.0 MHz
Storage Temperature Range	-55	-	+95	°C	

Note: ¹ Place a 10nF power supply bypass capacitor next to device for correct operation

² Typical capabilities shown. A unique OeXO® datasheet is created for each specific device. See Factory for other options.

Electrical Characteristics for Clipped Sine Wave

Parameter	Min	Typ	Max	Unit	Condition (Consult factory for other options)
Frequency Range ²	8.192	-	40.0	MHz	See table below for developed frequencies
Frequency Stability vs. Temperature ²	-200 -100 -50	-	+200 +100 +50	ppb	Over -40°C to +85°C Over -10°C to +70°C Over 0°C to +70°C at fixed V _{CC} + load (reference to midpoint min/max frequency) See factory for other options
Frequency Initial Calibration		-	±2.0	ppm	Vcontrol 1.50 volts at 25°C ± 2°C when V _{CC} ≥ 2.8 volts If Vcontrol used
Operating Temperature Range ²	-40	-	+85	°C	Widest range available
Supply Voltage ^{1,2} V _{CC}	2.8	-	3.3	Volts	± 5%
Supply Current ² I _{CC}	-	2.0 3.0 4.0	-	mA	13 MHz 26 MHz 40 MHz Load: 10 Kohm 10 pF, V _{CC} ± 5%
Frequency Stability vs. Supply	-	-	±0.2	ppm	Load: 10 Kohm 10 pF, V _{CC} ± 5%
Frequency Stability vs. Load	-	-	±0.2	ppm	Load: 10 Kohm 10 pF ± 10%
Vcontrol Range	0.5	-	2.5	Volts	1.50 volts nominal for V _{CC}
Frequency Pullability ²	0	±8.0	±12.0	ppm	Positive Slope
Linearity	-	-	2.0	%	
Output Waveform	Clipped Sine Wave				Dc Coupled
Output Level	0.8	-	-	V p-p	Load: 10 Kohm 10 pF ± 10%
Startup Time	-	-	10.0	mS	Within ± 2.0 ppm of final frequency
Long Term Stability (Aging)	-	-	±1.0	ppm	Per year at 25°C ± 2°C
Phase Noise	100 Hz 1 kHz 10 kHz 100 kHz	-	-120 -134 -144 -145	-	dBc/Hz 25°C ± 2°C at 20.0 MHz
Jitter	-	0.6	-	pS	Frequency offset from carrier 12 kHz to 20 MHz, Typical performance at 20.0 MHz
Storage Temperature Range	-55	-	+95	°C	

Note: ¹ Place a 10nF power supply bypass capacitor next to device for correct operation
² Typical capabilities shown. A unique OeXO® datasheet is created for each specific device. See Factory for other options.

The following is a list of developed frequencies. Consult factory for other options.

8.192M, 9.60M, 9.72M, 10.00M, 12.80M, 13.00M, 16.384M,
19.20M, 19.44M, 20.00M, 25.60M, 26.00M, 40.00M only

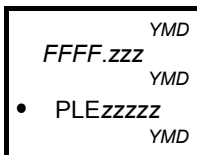
Part Number (Possible Options shown)

Series Model	V _{CC} Supply Voltage ¹	Operating Temperature		Stability ^{1,2}	Pullability ¹	Frequency
		Lowest	Highest	(ppm)	(ppm)	(MHz)
OED4	A unique number will be assigned for your exact specification					-19.44M
	3.3 volts nominal 3.0 volts nominal 2.8 volts nominal	+10°C +5°C +0°C -5°C -10°C -15°C -20°C -25°C -30°C -35°C -40°C	+40°C +45°C +50°C +55°C +60°C +65°C +70°C +75°C +80°C +85°C	± 0.05 ± 0.1 ± 0.2 ± 0.5 ± 1.0	0 ± 5 ± 8	10 - 40 MHz Developed: 8.192M, 9.60M, 9.72M, 10.00M, 12.80M, 13.00M, 16.384M, 19.20M, 19.44M, 20.00M, 25.60M, 26.00M, 40.00M

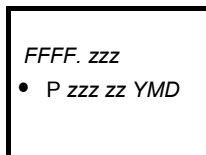
¹ Contact Factory for non-standard specifications

² Not all stabilities are available with all operating temperature ranges. Contact Factory for exact combinations available.

Device Marking



OR



FFFF = Crystal Frequency in MHz (See Note below)

z = Internal factory codes

PLE = Pletronics

YMD = Date code (may appear in one of 3 locations shown)

Note: Output Frequency may be half the Crystal Frequency marking, depending on requirements.

Specifications such as part number, frequency stability, supply voltage and operating temperature range, etc. are not identified from marking. External packaging labels and packing list will correctly identify the ordered Pletronics part number.

Codes for Date Code YMD (Year Month Day)

Code	6	7	8	9	0	Code	A	B	C	D	E	F	G	H	J	K	L	M
Year	2016	2017	2018	2019	2020	Month	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC

Code	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	X	Y	Z
Day	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Package Labeling

Tape and Reel available for quantities of 250 to 1000 per reel, cut tape for < 250. 16mm tape, 8mm pitch.

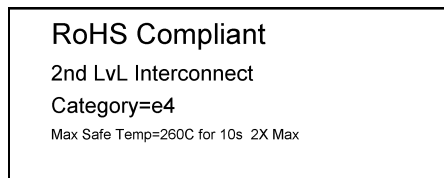
P/N Label is 1" x 2.6" (25.4mm x 66.7mm)

Font is Courier New

Bar code is 39-Full ASCII

RoHS Label is 1" x 2.6" (25.4mm x 66.7mm)

Font is Arial



Pletronics Inc. certifies this device is in accordance with the RoHS 2 (2011/65/EU) and WEEE (2002/96/EC) directives.

Pletronics Inc. guarantees the device does not contain the following: Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's

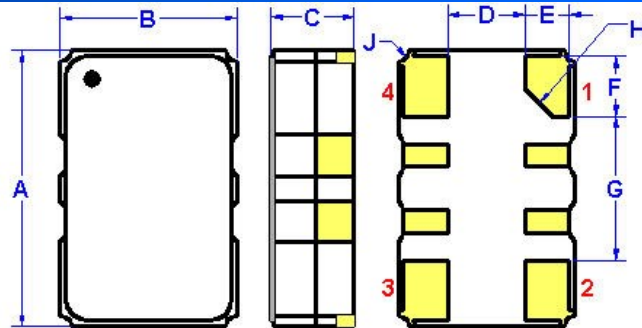
Weight of the Device: 0.10 grams

Moisture Sensitivity Level: 1 As defined in J-STD-020D

Second Level Interconnect code: e4

Mechanical Dimensions

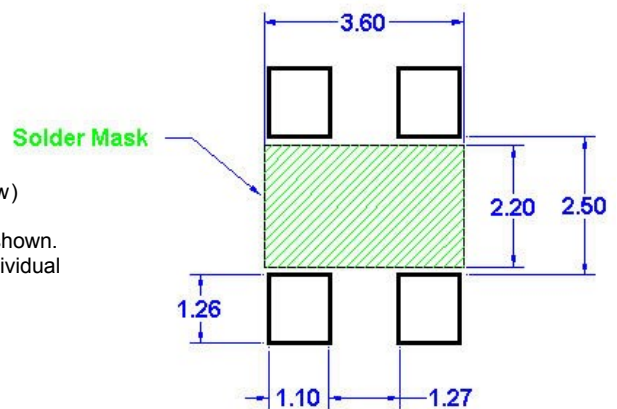
	Inches	mm
A	0.197 ± 0.008	5.00 ± 0.20
B	0.126 ± 0.008	3.20 ± 0.20
C	0.059 max	1.50 max
D ¹	0.055	1.40
E ¹	0.031	0.80
F ¹	0.043	1.10
G ¹	0.102	2.60
H ¹	0.020C	0.50C
J ¹	0.008R	0.20R



¹ Typical dimensions

Pad Layout mm shown (Top View)

Disclaimer: Recommended layout shown.
Adjust pad layout as needed for individual
process requirements.
Solder mask required, as shown.



(Not to Scale)

Contacts (pads): Gold 11.8 to 39.4 μinches (0.3 to 1.0 μm) over Nickel 50 to 350 μinches (1.27 to 8.89 μm)

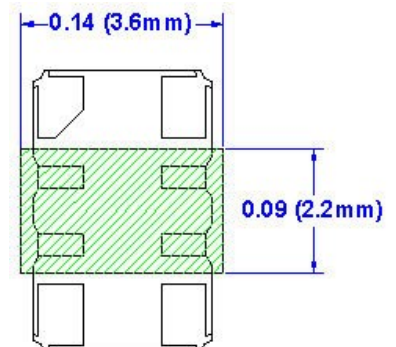
Layout

Pad	Function	Note
1	Vcontrol Input	If this function is not specified, recommend connecting this pad to ground. EFC (Electronic Frequency Control).
2	Ground (GND)	
3	Output	CMOS or Clipped Sine Wave (output is DC coupled. Most commonly used with external coupling capacitor. 0.001 to 0.01 μF recommended)
4	V _{CC} Supply Voltage	Connect an appropriate 10nF power supply bypass capacitor as close as possible
-	N.C.	All other pads on the bottom shall not be connected. These are internally connected for the TCXO compensation process

All connection points in the designated region have solder mask cover to avoid any electrical connections (top view shown)

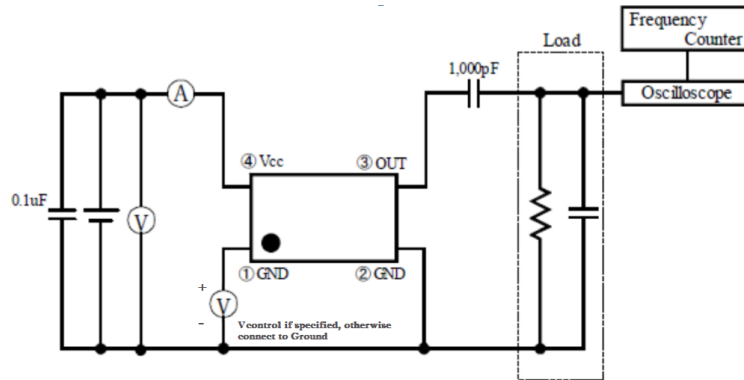
For Optimum Jitter Performance, Pletronics recommends:

- A ground plane under the device
- Do not route large transient signals (both current and voltage) under the device
- Do not place near a large magnetic field such as a high frequency switching power supply
- Do not place near piezoelectric buzzers or mechanical fans
- Minimize air flow across the device

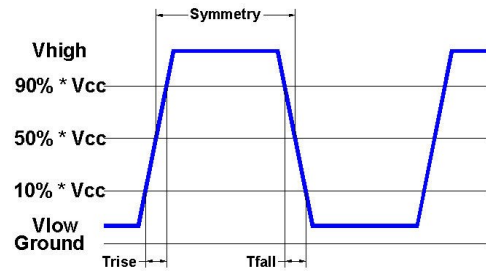
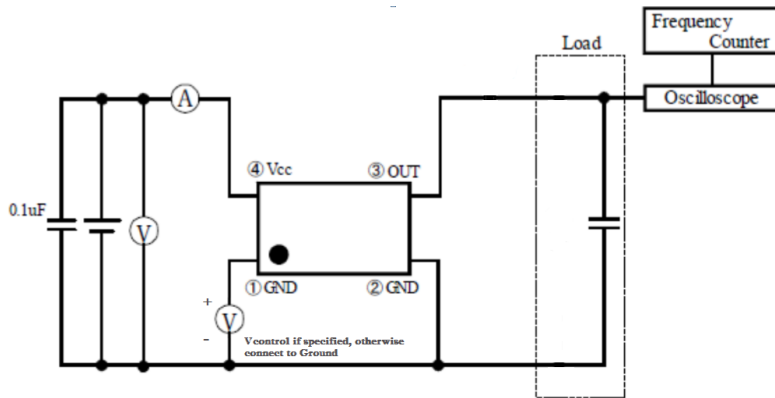


Electrical Test /Load Circuit

Clipped Sine Wave



CMOS



Environmental / ESD Ratings

Reliability: Environmental Compliance

Parameter	Condition
Mechanical Shock	JESD22-B104
Vibration	JESD22-B103
Solderability	IPC J-STD-002
Thermal Shock	MIL-STD-883 Method 1011, Condition A

ESD Rating

Model	Min. Voltage	Condition
Human Body Model	2000V	JESD22-A114
Charged Device Model	500V	JESD 22-C101
Machine Model	200V	JESD22-A115

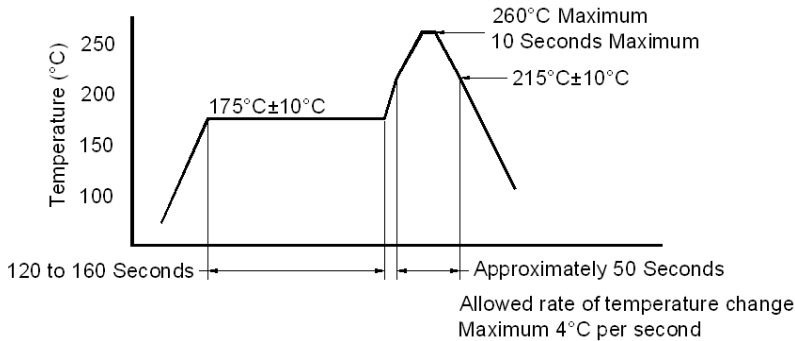
Absolute Maximum Ratings

Parameter	Unit
V _{CC} Supply Voltage	-0.6V to +6V
V _i Input Voltage	-0.6V to V _{CC} + 0.6V
I _o Output Current	-10mA to +10mA

Thermal Characteristics:

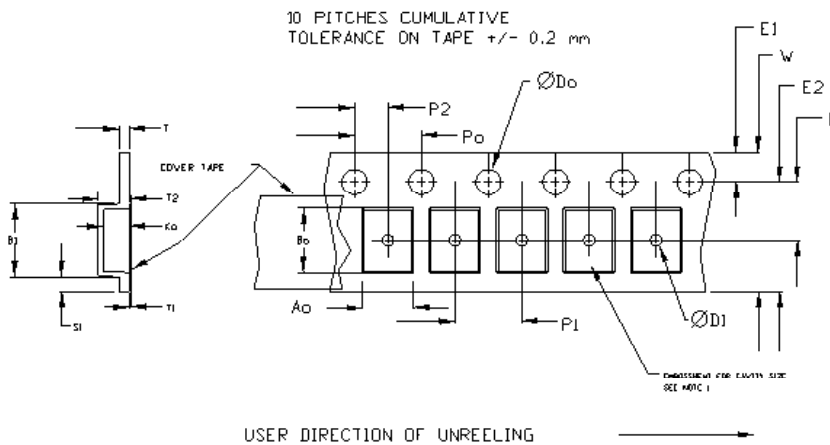
The maximum die or junction temperature is 155°C
The thermal resistance junction to board is 30 to 50°C/Watt depending on the solder pads, ground plane and construction of the PCB.

Reflow Cycle



The part may be reflowed 2 times without degradation (typical for lead free processing).

Tape and Reel

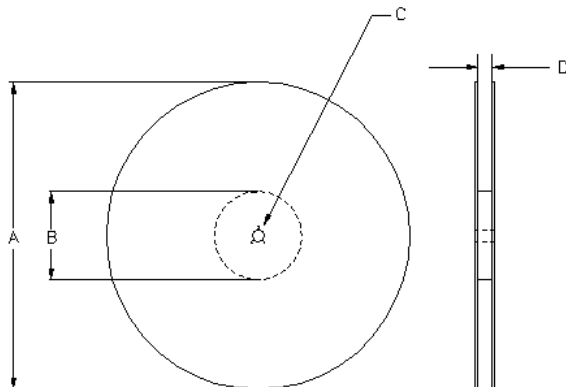


Tape Size	Do	D1 min	E1	Po	P2	S1 min	T max	T1 max
8mm	1.5	1.0	1.75	4.0	±0.05	0.6	0.6	0.1
12mm		1.5						
16mm		1.5						
24mm	+0.1 -0.0	1.5	±0.1	±0.1	±0.1			

Tape Size	B1 max	E2 min	F	P1	T2 max	W max	Ao, Bo & Ko
16mm	12.1	14.25	7.5 ±0.1	8.0 ±0.1	8.0	16.3	Note 1

Dimensions in mm Drawing Not to scale

Note 1: Embossed cavity to conform to EIA-481-B



Reel Size	A		B		C	D
	Inches	mm	Inches	mm		
7	7.0	177.8	2.50	63.5	13.0 +0.5 -0.2	Tape size +0.4 +2.0 -0.0
10	10.0	254.0	4.00	101.6		
13	13.0	330.2	3.75	95.3		

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