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- Pletronics' P113SD Series is a quartz crystal controlled precision square wave generator with a CMOS output.
- The P113SD series will directly interface TTL devices also.
- Greatly reduces RFI and EMI system sensitivity
- Minimizes RFI radiation, eases meeting FCC Class B emissions standards.
- Capable of driving up to 30pF capacitive loads
- Tube packaging is available.

- 70 to 107 MHz
- Full Size Thru-Hole DIP package
- Enable/Disable Function
- Disable function includes low standby power mode
- 3<sup>rd</sup> Overtone Crystals used
- Improved circuit to minimize oscillator issues such as multi-mode output signal.
- Low Jitter
- Has internal bypass capacitor on the Vcc lead
- 5x7 mm LCC ceramic oscillator inside

### Pletronics Inc. certifies this device is in accordance with the RoHS (2002/95/EC) and WEEE (2002/96/EC) directives.

Pletronics Inc. guarantees the device does not contain the following: Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's

Weight of the Device: 4.0 grams

Moisture Sensitivity Level: 1 As defined in J-STD-020C

Second Level Interconnect code: e1 or e2

#### **Absolute Maximum Ratings:**

Parameter	Unit
V <sub>cc</sub> Supply Voltage	-0.5V to +7.0V
Vi Input Voltage	0.5V to V <sub>cc</sub> + 0.5V
Vo Output Voltage	-0.5V to V <sub>CC</sub> + 0.5V

#### **Thermal Characteristics**

The maximum die or junction temperature is 155°C

The thermal resistance junction to board is 120°C/Watt depending on the solder pads, ground plane and construction of the PCB.



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#### **Part Number:**

P11	45	-3SD	ES	-100.0M	-30	-XX		Marking
							Internal code or blank	
							Output Load Capacitance Blank = 15pF maximum 30 = 30pF maximum	none
							Frequency in MHz	fff.fff M
							Supply Voltage V <sub>cc</sub> Blank = 5.0V ± 10%	none
							Enhanced Specifications (apply in the order shown) E = Temperature range -40 to 85°C S = Symmetry 45%/55% at 50% of V <sub>CC</sub>	E S
							Series Model	
						Á	Frequency Stability  45 = ± 50 ppm  44 = ± 25 ppm  20 = ± 20 ppm	5 4 2
							Series Model	P3S

### Part Marking:

PLE
P3Sxss

ss = Enhanced specification

fff.fff M
yywwaLF

Where: x = Frequency stability

= Enhanced specification

fff.fff = Frequency in MHz

yywwa = Date code

LF = Lead Free

(Voltage not shown)

Pletronics may ship the following combinations without notice (this is an enhanced specified device)

- 44 (25 ppm) stability parts when 45 (50 ppm) was ordered
- 20 (20 ppm) stability parts when 45 (50 ppm) or 44 (25 ppm) was ordered.
- E temperature range parts when extended was not ordered.
- S symmetry parts when 40/60% symmetry was ordered.

Pletronics may ship parts that are not marked for extended temperature range but were tested for extended temperature range, a Certificate of Conformance will accompany these parts.

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### Electrical Specification for $5.00V \pm 10\%$ over the specified temperature range

Item	Min	Max	Unit	Condition
Frequency Range	70	107	MHz	
Frequency Accuracy "45"	-50	+50	ppm	For all supply voltages, load changes, aging for 1
" <b>44</b> "	-25	+25		year, shock, vibration and temperatures
<b>"20"</b>	-20	+20		
Output Waveform	CMOS			
Output High Level	0.5	-	V	Below V <sub>CC</sub> (See load circuit)
Output Low Level	1	0.4	V	(See load circuit)
Output Symmetry	40	60	%	at 50% point of V <sub>cc</sub> (See load circuit) Standard
	45	55	%	for "S" option parts
Jitter	-	1	pS RMS	12 KHz to 20 MHz from the output frequency
	-	4	pS RMS	10 Hz to 1 MHz from the output frequency
Enable/Disable Internal Pull-up	50	-	Kohm	to V <sub>cc</sub>
V disable	1	0.5	>	Applied to pad 1
V enable	2.0	\[ \frac{1}{2} \]	>	Applied to pad 1
Output leakage $V_{OUT} = V_{CC}$	-10	+10	uA	Pad 1 low, device disabled
$V_{OUT} = 0V$	-10	+10	uA	
Enable time	J	100	nS	Time for output to reach a logic state
Disable time	<b>/</b>	100	nS	Time for output to reach a high Z state
Start up time	1	10	mS	Time for output to reach specified frequency
Operating Temperature Range	0	+70	°C	Standard Temperature Range
	-40	+85	°C	Extended Temperature Range "E" Option
Storage Temperature Range	-55	+125	°C	





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### Electrical Specification for 5.00V ±10% over the specified temperature range

Item	Min	Тур	Max	Unit	Condition
V <sub>OUT</sub> High (V <sub>OH</sub> )	0.5	0.3	-	V	Below V <sub>CC</sub> , I <sub>OH</sub> = +16 mA
V <sub>OUT</sub> Low (V <sub>OL</sub> )	-	0.3	0.4	V	I <sub>OL</sub> = -16 mA
Output T <sub>RISE</sub> and T <sub>FALL</sub>	-	2.0	4.0	nS	C <sub>LOAD</sub> = 15 pF,
	-	3.0	6.0	nS	C <sub>LOAD</sub> =30 pF,
V <sub>cc</sub> Supply Current	-	50	90	mA	>100 MHz
(I <sub>cc</sub> )	-	45	80	mA	<=100 MHz 10% to 90% of V <sub>cc</sub> (See load circuit)
	-	60	100	mA	>100 MHz C <sub>LOAD</sub> = 30 pF
	-	50	100	mA	<=100 MHz 10% to 90% of V <sub>CC</sub> (See load circuit)

Specifications with Pad 1 E/D open circuit

#### **Load Circuit and Test Waveform** Symmetry Vhigh 90% \* Vcc-50% \* Vcc 0.01 uF UUT 10% \* Vcc Vlow Ground GND To oscilloscope and counter 5K ohm minimum C LOAD maximum per specification All leads 0.2 inches (5mm) or less

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#### Reliability: Environmental Compliance

Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002, Condition A
Vibration	MIL-STD-883 Method 2007, Condition A
Solderability	MIL-STD-883 Method 2003
Thermal Shock	MIL-STD-883 Method 1011, Condition A



Model	Minimum Voltage	Conditions
Human Body Model	1500	MIL-STD-883 Method 3115
Charged Device Model	1000	JESD 22-C101

#### **Package Labeling**

Label is 1" x 2.6" (25.4mm x 66.7mm) Font is Courier New Bar code is 39-Full ASCII



Label is 1" x 2.6" (25.4mm x 66.7mm) Font is Arial

#### Pb Free

2nd LvL Interconnect Catagory=e1

Max Safe Temp=280C for 15s (Wave solder only)
Max Safe Temp=245C for 10s (Reflow only)

#### Pb Free

2nd LvL Interconnect Catagory=e2

Max Safe Temp=280C for 15s (Wave solder only)
Max Safe Temp=245C for 10s (Reflow only)

### PCB Mounting (typical for lead free processing)

Hand soldering is recommended.

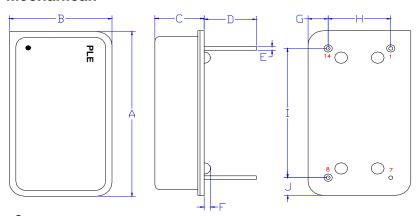
Wave solder at 255°C to 280°C with maximum wave exposure of 15 seconds Reflow solder maximum exposure of 245°C for 15 seconds Soldering done in a nitrogen atmosphere enhances the solder joint quality.

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#### Mechanical:



Cover:

Kovar

Electroless Nickel Plated 1 µinch (25 µm) typical Resistance welded to base

Label:

White Kapton with Black Letters

Blue Epoxy heat cure ink with laser marked lettering

Base:

Kovar

Glass to metal sealed leads.

Pin 7 Connected to case

Not to scale

	Inches	mm
Α	0.787 <u>+</u> 0.005	20.00 ±0.13
В	0.487 <u>+</u> 0.005	12.37 <u>+</u> 0.13
С	0.225 <u>+</u> 0.011	5.72 ±0.28
D¹	0.250	6.35
E¹	0.020	0.51
F <sup>1</sup>	0.031	0.79
G <sup>1</sup>	0.094	2.37
工	0.300	7.62
l¹	0.600	15.24
J <sup>1</sup>	0.094	2.37

<sup>1</sup> Nominal dimension

Pad	Function	Note
1	Output Enable/Disable	When this pad is not connected the oscillator shall operate. When this pad is logic low the output will be inhibited (high impedance state.) Recommend connecting this pad to $V_{\rm cc}$ if the oscillator is to be always on.
7	Ground (GND)	
8	Output	
14	Supply Voltage (V <sub>cc</sub> )	Recommend connecting appropriate power supply bypass capacitors as close as possible.

### Layout and application information

For Optimum Jitter Performance, Pletronics recommends:

- a ground plane under the device
- no large transient signals (both current and voltage) should be routed under the device
- do not layout near a large magnetic field such as a high frequency switching power supply
- do not place near piezoelectric buzzers or mechanical fans.



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#### IMPORTANT NOTICE

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